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(54) Data sensing device and method for multibit memory cell

(57) Data sensing device and method for a multibit memory cell is disclosed, the device including a reference voltage generating part (1) for generating a plurality of reference voltages, a switching part (2) for successive application of the plurality of reference voltages from the reference voltage generating part (1) to a control gate on a memory cell (3), a sensing part (4) for comparing a data recorded in the memory cell (3) to the reference value every time each of the reference voltages is applied thereto, a clock signal controlling part (5) for subjecting a signal from the sensing part (4) and a highest reference voltage selecting signal to logical operation in controlling an external main clock signal, a controlling part (6) for controlling the switching part (2) to generate the reference voltages in succession, and controlling a highest reference voltage to be applied to the clock signal controlling part (5) so that the data is produced in response to a clock signal from the clock signal controlling part (5), and a latching part (7) for latching the data from the controlling part (6).

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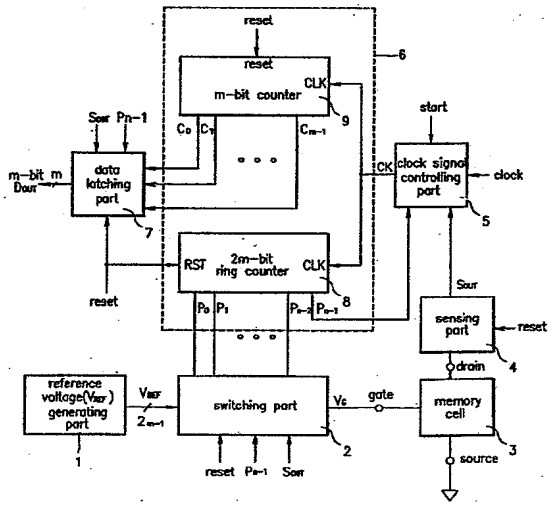

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to device and method for reading in information stored in a semiconductor device and, more particularly, to a data sensing device and method for a multibit memory cell for reading in a data programmed in multilevel of two or over two levels stored in the multibit memory cell.

Discussion of the Related Art

In the semiconductor memories, in general, there are at large volatile memories from/to which information is erasable and recordable, and non-volatile memories information once recorded in which can be conserved permanently. In the volatile memories, there RAM to/from which data is recordable and readable, and in the non-volatile memories, there are ROM, EPROM(Erasable Programmable ROM) and EEPROM(Electrically Erasable Programmable ROM). Of the non-volatile memories, the ROM is a memory which is no more programmable once information is recorded, and both the EPROM and EEPROM are memories from/to which information is erasable and recordable. The EPROM and EEPROM are identical in their programming operations, but different in their information erasing operations; the information recorded in EPROM is erased by an ultra-violet beam and the information stored in EEPROM is electrically erased.

Of those memories, the DRAM is the most widely used as a mass storage media because large sized memories are required as the information industry is developed. However, the DRAM, which requires a storage capacitor of greater than a predetermined size, has a disadvantage that refreshing operations of the capacitor are required in certain intervals due to the use of capacitor. Because of this, there has been ceaseless study on the EEPROM, which does not require any refreshing operations, in substitution for the DRAM. However, since the EEPROM can also store data of either "1" or "0" in a memory cell, device packing density corresponds to a number of the memory cells in one to one fashion. Therefore, the drawback in using the EEPROM as a data storage media that is the most difficult to overcome is the high cost-per-bit of the memories.

In order to solve such a problem, active studies on multibit-per-cell are currently underway. A multibit memory cell stores data of over two bits in one memory cell, thus enhancing the density of data on the same chip area without reducing the size of the memory cell. For the multibit memory cell, more than two threshold voltage levels should be programmed on respective cell. For instance, in order to store data of two bits for every cell, the respective cells must be programmed in 2^2, that is, four threshold levels. Here, the four threshold levels corresponds to logic states 00, 01, 10 and 11, respectively. As distribution is reduced by precisely adjusting the respective threshold levels, more levels can be programmed, which in turn increases the number of bits for every cell. The data thus programmed in multilevels should be read in fast speed.

A conventional data sensing device for sensing a memory cell programmed in such a multilevels will be explained with reference to the attached drawing. Fig. 1 illustrates a system of a conventional sensing device for sensing a multibit memory cell, and Fig. 2 illustrates a graph explaining the operation of the conventional sensing device for sensing a multibit memory cell. When voltages sufficient to cause reading are applied to a control gate, a current flows between a drain and a source. The current is compared to a reference current and determined of the data in reading the multilevel data. Referring to Fig. 1, a system is provided having a sensing amplifier(S.A) connected to a drain region D in a unit cell of an EEPROM with a floating gate F.G., control gate C.G., source region S and the drain region D. The sensing amplifier S.A. has a plurality of reference currents therein.

A method of sensing the data in the conventional multibit memory cell having the aforementioned system will be explained.

It is assumed that the memory cell has been programmed in multilevel threshold voltages. That is, as shown in Fig. 2, in case of recording a two bit data, it is assumed that the two bit data has been programmed in the floating gate F.G. as one of four threshold voltages V_{T0}, V_{T1}, V_{T3}, V_{T4}. Under the condition that a constant voltage is applied to the source region S, a predetermined voltage V_{READ} is selectively applied to the control gate C.G. of a memory cell of which data is intended to read. Then, according to the programmed state in the floating gate F.G., a drain current I_D corresponding to the programmed state flows through the sensing amplifier S.A. The sensing amplifier S.A. compares the drain current from the memory cell to the multilevel reference currents within the sensing amplifier S.A in multilevels, thereby the data can be read. That is, referring to Fig. 2, if the floating gate F. G. of a memory cell in an EEPROM from which a data is intended to read has been programmed in the threshold voltage V_{T0}, a drain current I_{R0} corresponding to the threshold voltage V_{T0} will flow through the sensing amplifier S.A., if the floating gate F. G. has been programmed in the threshold voltage V_{T1}, a drain current corresponding to the threshold voltage V_{T1} will flow through the sensing amplifier S.A., and if the floating gate F. G. has been programmed in the threshold voltage V_{T2}, a drain current corresponding to the threshold voltage V_{T2} will flow through the sensing amplifier S.A. Therefore, upon reception of the drain current from the drain of the memory cell, the sensing amplifier S.A. can sense the data by comparing the drain current with the multilevel reference currents

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within the sensing amplifier SA.

However, the conventional data sensing device and method for sensing a data in a multibit memory cell has the following problems because a predetermined voltage Vc of a readable condition is applied to the control gate of a memory cell from which a data is intended to read in selection of the memory cell, and the drain cuffent from the memory cell is compared in multilevels in the sensing amplifier in reading the data.

First, for the multilevel comparison of the current from the memory cell by the sensing amplifier in reading the data, the sensing amplifier must have the multilevel reference currents, that causes the size of the sensing amplifier bigger, particularly in a page mode READ, in which more bits(for example, 512 bits, 128 bits) are required, together with chip size.

Second, the plurality of reference currents always required to supply to the sensing amplifier causes increase of power consumption.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a data sensing device and method of a multibit memory cell that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, the data sensing device of a multibit memory cell includes a reference voltage generating part for generating a plurality of reference voltages, a switching part for successive application of the plurality of reference voltages from the reference voltage generating part to a control gate on a memory cell, a sensing part for comparing a data recorded in the memory cell to the reference value every time each of the reference voltages is applied thereto, a clock signal controlling part for subjecting a signal from the sensing part and a highest reference voltage selecting signal to logical operation in controlling an external main clock signal, a controlling part for controlling the switching part to generate the reference voltages in succession, and controlling the highest voltage to be applied to the clock signal controlling part so that the data is produced in response to a clock signal from the clock signal controlling part, and a latching part for latching the data from the controlling part.

In another aspect of the present invention, there is provided a method for sensing a data in a multibit memory cell including the steps of receiving an external main clock signal, successive latching of data in response to the main clock signal, successive application of a plurality of reference voltages to a control gate on a memory cell, sensing the memory cell whenever each of the reference voltages is applied to the memory cell, detecting a time when an output of the sensing part is changed for blocking the main clock signal, and presenting a data latched by a most recent clock signal as a programmed data in the memory cell.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the drawings:

In the drawings:

Fig. 1 illustrates a system of a conventional sensing device for sensing a multibit memory cell;

Fig. 2 illustrates a graph for use in explaining the operation of the conventional sensing device for sensing a multibit memory cell;

Fig. 3 illustrates a block diagram of a device for sensing a data in a multibit memory cell in accordance with a first embodiment of the present invention;

Fig. 4 illustrates a detail circuit of a first embodiment of the switching part shown in Fig. 3;

Fig. 5 illustrates a detail circuit of a second embodiment of the switching part shown in Fig. 3;

Fig. 6 illustrates a detail circuit of the clock signal controlling part shown in Fig. 3;

Fig. 7 illustrates a detail circuit of the latching part shown in Fig. 3;

Fig. 8 illustrates a block diagram of a device for sensing a data in a multibit memory cell in accordance with a second embodiment of the present invention;

Fig. 9 explains threshold levels of an n bit cell and the corresponding reference voltages in accordance with the present invention;

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Fig. 10 explains reference voltage selection in the first embodiment of the present invention;

Fig. 11 explains reference voltage selection in the second embodiment of the present invention;

Fig. 12 explains timings of different parts when the memory cell of the present invention is programmed in a threshold level V_{TH2}; and,

Fig. 13 explains timings of different parts when the highest level data is read according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

Fig: 3 illustrates a block diagram of a device for sensing a data in a multibit memory cell in accordance with a first embodiment of the present invention.

Referring to Fig. 3, the device for sensing a data in a multibit memory cell in accordance with a first embodiment of the present invention includes a reference voltage generating part 1 for generating a plurality of reference voltages(2^n-1 in case of n bits), a switching part 2 for applying the plurality of reference voltages from the reference voltage generating part 1 to a control gate in a memory cell 3 in succession under the control of the controlling part which will be explained later, a sensing part 4 for comparing the data recorded in the memory cell 3 having one of the reference voltage applied thereto to a reference value, a clock signal controlling part 5 for receiving a signal from the sensing part 4 and a highest voltage selection signal from a controlling part which will be explained below and subjecting to logical operation in controlling an external main clock signal, a controlling part 6 for applying a reference voltage selection signal to the switching part 2 to control the reference voltages generated in succession(in the order of from a lower reference voltage to a higher reference voltage or vice versa) and producing a data in response to a clock signal from the clock signal controlling part 5, and a data latching part 7 for latching the data from the controlling part 6.

The controlling part 6 includes a ring counter 8 for counting the clock signal from the clock signal controlling part 5 in generating the reference signal selection signals P_0, P_1 --- P_{n-2}, and P_{n-1}, and an n-bit counter 9 for counting the clock signal from the clock signal controlling part 5 in producing a relevant data.

Detailed circuits of the aforementioned device for sensing a data in a multibit memory cell will be explained. Fig. 4 illustrates a detail circuit of a first embodiment of the switching part shown in Fig. 3, Fig. 5 illustrates a detail circuit of a second embodiment of the switching part shown in Fig. 3, Fig. 6 illustrates a detail circuit of the clock signal controlling part shown in Fig. 3, and Fig. 7 illustrates a detail circuit of the latching part shown in Fig. 3.

Referring to Fig. 4, the switching part 1 includes a plurality of transistors M_1, M_2, ---, M_{n-1} each for switching the plurality of reference voltages from the reference voltage generating part 1 in succession in response to the reference voltage selection signals P_0, P_1, P_2, --- and P_{n-2} except the highest reference voltage selection signal P_{n-1} of the reference voltage selection signals P_0, P_1 --- P_{n-2}, and P_{n-1} from the controlling part 6, an OR gate IC_1 for subjecting the highest reference voltage selection signal P_{n-1} from the controlling part 6, a signal S_{OUT} from the sensing part 4 and a reset signal RESET to a logical sum operation, and a transistor Q_1 for switching the reference voltages applied to an output terminal thereof from the plurality of transistors M_1, M_2, ---, M_{n-1} in response to a signal from the OR gate IC_1. The switching part 2 may include a plurality of pass transistors PTR_1 as shown in Fig. 5 in place of the plurality of transistors M_1, M_2, ---, M_{n-1} shown in Fig. 4, each of which produces the reference signal at "high".

Referring to Fig. 6, the clock signal controlling part 5 includes an NOR gate IC_2 for subjecting the highest reference voltage selection signal P_{n-1} from the controlling part 6 and the signal S_{OUT} from the sensing part 4 to a logical sum operation and inverting a resultant of the logical sum operation, and an AND gate IC_3 for subjecting a start signal START, external main clock signal CLOCK and a signal from the NOR gate IC_2 to a logical production operation in applying the clock signal to the controlling part 6.

Referring to Fig. 7, the latching part 7 includes a plurality of flipflops. That is, the latching part 7 includes a delay D_1 for delaying the highest reference voltage selection signal P_{n-1} for a predetermined time period, an OR gate IC_4 for subjecting a signal from the delay D_1 and the signal S_{OUT} from the sensing part 4 to a logical sum operation, and the plurality of flipflops F/F_0, F/F_1, ---, F/F_{n-1} for latching the data from the n-bit counter 9 in the controlling part 6 using a signal from the OR gate IC_4 as a clock signal.

Fig. 8 illustrates a block diagram of a device for sensing a data in a multibit memory cell in accordance with a second embodiment of the present invention.

Referring to Fig. 8, the device for sensing a data in a multibit memory cell in accordance with a second embodiment of the present invention has a decoder 8a for decoding the plurality of reference signal selection signals in place of the ring counter 8 in the controlling part 6 of the device for sensing a data in a multibit memory cell in accordance with the first embodiment of the present invention.

A sensing method in the device for sensing a data in a multibit memory cell in accordance with the present invention will be explained.

Fig. 9 explains threshold levels of an n bit cell and

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the corresponding reference voltages in accordance with the present invention, Fig. 10 explains reference voltage selection in the first embodiment of the present invention, and Fig. 11 explains reference voltage selection in the second embodiment of the present invention.

A value between adjacent threshold levels is taken as the reference voltage. For example, if the threshold levels are 2, 4, 6, 8, the reference voltages may be 3, 5, 7. Accordingly, the reference voltage generating part 1 generates 2^n-1 number of voltages each corresponding to an intermediate value of adjacent threshold voltage levels in case of an n bit memory cell. The controlling part 6 controls the switching part 2 to output the reference voltages from the reference voltage generating part 1 in succession. In this instance, if the threshold levels are n bits, though a 2^n-1 number of reference voltages is required, a number of the reference voltage selection signals from the controlling part 6 is 2^n. Therefore, the reference voltages are actually selected by the reference voltage selection signals P_0, P_1, P_2, --- and P_{n-2}, but the highest reference voltage selection signal P_{n-1}. That is, the controlling part 6 controls the switching part 2 to output the reference voltages in an order of from a lower voltage to a higher voltage as shown in Fig. 10, or from a higher voltage to a lower voltage as shown in Fig. 11, by the following method.

When the ring counter 8 or the decoder 8a in the controlling part 8 generates the high reference voltage selection signals in the order of from P_0 to P_{n-1}, the transistors M_1, M_2, ---, M_{n-1} in the switching part 2 having the high signals applied thereto are turned on to output the reference voltages in the order of from a lower voltage to a higher voltage as shown in Fig. 10. In this instance, of the reference voltage selection signals from the controlling part 6, the highest reference voltage selection signal P_{n-1} is applied, not to any of the transistors in the switching part 2, but to the OR gate IC_1 in the switching part 2, clock signal controlling part 5 and the latching part 7. Therefore, in case the reference voltages are produced in the order of from lower reference voltage to higher reference voltage as shown in Fig. 10, the highest reference voltage is produced by the reference voltage selection signal P_{n-2}. Oppositely, when the ring counter 8 or the decoder 8a in the controlling part 8 generates the high reference voltage selection signals in the order of from P_{n-2} to P_0, and the P_{n-1} finally, the transistors M_1, M_2, ---, M_{n-1} in the switching part 2 having the high signals applied thereto are turned on to output the reference voltages in the order of from a higher voltage to a lower voltage as shown in Fig. 11. For reduction of power consumption, it is preferable to produce the reference voltages in the order of from lower reference voltage to higher reference voltage as shown in Fig. 10, because, at reading data, the data may be sensed, not always by selecting up to the last reference voltage, but by selecting an intermediate reference voltage.

When the reference voltages are thus applied from the switching part 2 to the control gate on the memory cell 3 in succession, the sensing part makes turning on/off operations. In this instance, a channel is formed between a source region and a drain region in the memory cell 3 in case a reference voltage over a threshold level is applied to the control gate, and no channel is formed between the source region and the drain region in the memory cell 3 in case a reference voltage below a threshold level is applied to the control gate. Accordingly, the sensing part 4 also produces a high signal when a reference voltage over a threshold level is applied to the control gate, and a low signal when a reference voltage below a threshold level is applied to the control gate. For explaining it in detail, it is assumed that the controlling part 6 applies the reference voltages to the control gate on the memory cell 3 in the order of from lower reference voltage to higher reference voltage as shown in Fig. 10, the memory cell has been programmed in one of the two bit threshold levels $V_{TH,0}$, $V_{TH,1}$, $V_{TH,2}$ and $V_{TH,3}$, and there are three of the reference voltages $V_{REF,0}$, $V_{REF,1}$ and $V_{REF,2}$ each of which value falls on between adjacent two of the threshold levels. Upon the reference voltage $V_{REF,0}$ a is applied to the control gate on the memory cell 3 by the switching part 2, the sensing part 4 produces a high signal only when the memory cell has been programmed in the threshold level $V_{TH,0}$ because the channel will be formed between the source region and the drain region of the memory cell, and the sensing part 4 produces a low signal when the memory cell has been programmed in one of the rest of the threshold levels $V_{TH,1}$, $V_{TH,2}$ and $V_{TH,3}$. Alikely, upon the reference voltage $V_{REF,2}$ is applied to the control gate on the memory cell 3 by the switching part 2, the sensing part 4 produces a low signal only when the memory cell has been-programmed in the threshold level $V_{TH,3}$ because the channel will not be formed between the source region and the drain region of the memory cell, and the sensing part 4 produces a high signal when the memory cell has been programmed in one of the rest of the threshold levels $V_{TH,0}$, $V_{TH,1}$ and $V_{TH,2}$. By determining an output of the sensing part 4 whenever one of the reference voltages is applied to the control gate on the memory cell while elevating the reference voltage from the lowest voltage to the highest voltage in succession according to the aforementioned principle, and by counting a time point when the output of the sensing part 4 is changed to "high", the device of the present invention senses a data in the multibit memory cell.

A sensing method of the device for sensing a data in a multibit memory cell in accordance with the first embodiment of the present invention will be explained with reference to Figs. 12 and 13. Fig. 12 explains timings of different parts when the memory cell of the present invention is programmed in a threshold level V_{TH2}, and Fig. 13 explains timings of different parts when the highest level data is read according to the present invention.

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Upon reception of an external main clock signal CLOCK, then, a reset signal RESET and a start signal START, the clock signal controlling part 5 produces a clock signal to the controlling part 6. The controlling part 6 then counts the clock to generates a reference voltage selection signal and a 2 bit data signal. That is, the ring counter 8 in the controlling part 6 causes the lowest reference voltage $V_{REF, 0}$ a to be produced and applied to the memory cell 3 through the switching part 2, and the n bit counter 9 in the controlling part 6 produces a data 00. Upon reception of the reference voltage $V_{REF, 0}$ a thus, since the memory cell 3 is programmed in the threshold level $V_{TH,, 2}$, the sensing part 4 produces a low signal. As all of the signal S_{OUT} from the sensing part 4 and the reference voltage selection signal P_{n-1} from the controlling part 6 are at "low", the NOR gate IC_2 in the clock signal controlling part 6 produces a high signal, so that the AND gate IC_3 in the clock signal controlling part 5 continues to apply the external main clock signal CLOCK to the controlling part 6. The controlling part 6, counting the clock signal applied thereto continuously according to the aforementioned process, proceeds the next operation. That is, the controlling part 6 controls the ring counter 8 to produce the reference voltage selection signal P_1 at a second rising edge of the clock signal for producing the next reference voltage $V_{REF, 1}$, the reference voltage $V_{REF,1}$ produced in the reference voltage generating part 1 to be applied to the memory cell 3, and the n bit counter 9 to produce the data 01. Even if the reference voltage $V_{REF, 1}$ is received, the sensing part 4 produces a low signal because the memory cell 3 has been programmed in the threshold level $V_{TH, 2}$. As all of the signal S_{OUT} from the sensing part 4 and the reference voltage selection signal P_{n-1} from the controlling part 6 are at "low", the NOR gate IC_2 in the clock signal controlling part 6 produces a high signal, so that the AND gate IC_3 in the clock signal controlling part 5 continues to apply the external main clock signal CLOCK to the controlling part 6. Then, the controlling part 6 controls the ring counter 8 and the n bit counter 9 to cause the reference voltage $V_{REF, 2}$ generated in the reference signal generating part 1 to be applied to the memory cell 3 through the switching part 2 and to produce the data 10 respectively at a third rising edge of the clock signal. Upon reception of the reference voltage $V_{REF, 2}$, the sensing part 4 produces a high signal because the memory cell 3 has been programmed in the threshold level $V_{TH, 2}$. As the signal S_{OUT} from the sensing part 4 is the high signal, the NOR gate IC_2 in the clock signal controlling part 5 produces a low signal regardless of the reference voltage selection signal P_{n-1} from the controlling part 6. Therefore, the AND gate IC_3 in the clock signal controlling part 5 applies no external main clock signal CLOCK to the controlling part 6. If no clock signal is applied to the controlling part 6, all the parts of the sensing device are initialized, and the latching part 7 presents the data 10 finally produced in the n bit counter 9 of the controlling part 6 as a sensed data.

According to the aforementioned method, a 2^n-1 number of level values are sensed except the highest level value in the multilevel programmed memory cell, and the remained one highest level value is sensed by a method as shown in Fig. 13.

That is, if the memory cell has been programmed in the highest threshold level $V_{TH, 3}$, even if the controlling part 6 produces a reference voltage selection signal to apply the highest reference voltage $V_{REF, 2}$ to the memory cell 3, the sensing part 4 produces a low signal. When the sensing part 4 thus produces the low signal, the clock signal controlling part 5 also continues to apply the external clock signal to the controlling part 6. Then, the ring counter 8 and the n bit counter 9 in the controlling part 6 respectively count the clock signal to produce the highest reference voltage selection signal P_{n-1} at "high" and to apply the data 11 to the latching part 7 at a fourth rising edge of the clock signal, respectively. The NOR gate IC_2 in the clock signal controlling part 5 then produces a low signal to stop application of the external clock signal to the controlling part 6 even if the low signal is under production in the sensing part 4. According to the aforementioned method, the latching part 7 can present a final data 11.

On the other hand, the sensing method of the device for sensing a data in a multibit memory cell in accordance with the second embodiment of the present invention is identical to the sensing method of the device for sensing a data in a multibit memory cell in accordance with the first embodiment of the present invention, except the operation of the controlling part 6. That is, the decoder 8a in the second embodiment is applied of, not the clock signal from the clock signal controlling part 5, but the a data signal from the n bit counter 9, in decoding the reference voltage selection signal.

As has been explained, the data sensing device and method for a multibit memory cell of the present invention has the following advantages.

First, since data can be sensed by successive application of reference voltages to a control gate on a multilevel programmed memory cell, which facilitates the sensing amplifier to be merely required to determine generation of a voltage in the multibit memory cell, a size of the sensing amplifier can be minimized.

Second, the requirement for application of only one reference voltage of a certain value to the sensing amplifier helps to reduce a power consumption

It will be apparent to those skilled in the art that various modifications and variations can be made in the data sensing device and method for a multibit memory cell of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

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Claims

1. A device for sensing a data in a multibit memory cell comprising:

   a reference voltage generating pan for generating a plurality of reference voltages;

   a switching part for successive application of the plurality of reference voltages from the reference voltage generating part to a control gate on a memory cell;

   a sensing part for comparing a data recorded in the memory cell to the reference value every time each of the reference voltages is applied thereto;

   a clock signal controlling part for subjecting a signal from the sensing part and a highest reference voltage selecting signal to logical operation in controlling an external main clock signal;

   a controlling part for controlling the switching part to generate the reference voltages in succession, and controlling a highest reference voltage to be applied to the clock signal controlling part so that the data is produced in response to a clock signal from the clock signal controlling part; and,

   a latching part for latching the data from the controlling part.

2. A device as claimed in claim 1, wherein the controlling part includes,

   a ring counter for counting the clock signal from the clock signal controlling part in controlling production of the reference voltage selection signal in the switching part, and

   an n-bit counter for counting the clock signal from the clock signal controlling part in production of a relevant data.

3. A device as claimed in claim 2, wherein the controlling part includes a decoder for decoding the plurality of reference voltage selection signal in place of the ring counter.

4. A device as claimed in claim 1, wherein the switching part includes,

   a plurality of transistors for switching the plurality of reference voltages from the reference voltage generating part in succession in response to the reference voltage selection signals respectively except the highest reference voltage selection signal of the reference voltage selection signals from the controlling part,

   an OR gate for subjecting the highest reference voltage selection signal from the controlling part, a signal from the sensing part and a reset signal to logical sum operation, and

   a transistor for switching the reference voltages applied from the plurality of transistors to an output terminal thereof in response to a signal from the OR gate.

5. A device as claimed in claim 4, wherein the switching part may include a plurality of pass transistors in place of the plurality of transistors.

6. A device as claimed in claim 1, wherein the clock signal controlling part includes,

   an NOR gate for subjecting the highest reference voltage selection signal from the controlling part and the signal from the sensing part to logical sum operation and inverting a resultant of the logical sum operation, and

   an AND gate for subjecting a start signal, an external main clock signal and a signal from the NOR gate to logical production operation in applying the clock signal to the controlling part.

7. A device as claimed in claim 1, wherein the latching part includes,

   a delay for delaying the highest reference voltage selection signal for a predetermined time period,

   an OR gate for subjecting a signal from the delay and the signal from the sensing part to logical sum operation, and

   a plurality of flipflops for latching the data from the n-bit counter in the controlling part using a signal from the OR gate as a clock signal.

8. A method for sensing a data in a multibit memory cell comprising the steps of:

   (1) receiving an external main clock signal;

   (2) successive latching of data in response to the main clock signal;

   (3) successive application of a plurality of reference voltages to a control gate on a memory cell;

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(4) sensing the memory cell whenever each of the reference voltages is applied to the memory cell;

(5) detecting a time when an output of the sensing part is changed for blocking the main clock signal; and,

(6) presenting a data latched by a most recent clock signal as a programmed data in the memory cell.

9. A method as claimed in claim 8, wherein a number of the reference voltages produced is 2n-1 when the memory cell has been programmed in n bits, and the reference voltages are produced in an order of from a lower voltage to a higher voltage and data are latched in an order of from a higher data to a lower data.

10. A method as claimed in claim 8, further comprising the step of presenting a highest data as the programmed data in the memory cell if no output change time is detected in the (5) step even if the highest reference voltage is applied to the memory cell.

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FIG.1
conventional art

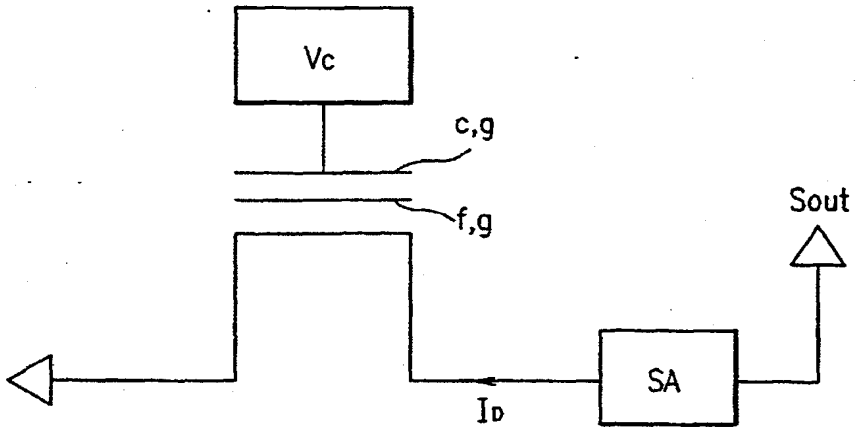

FIG.2
conventional art

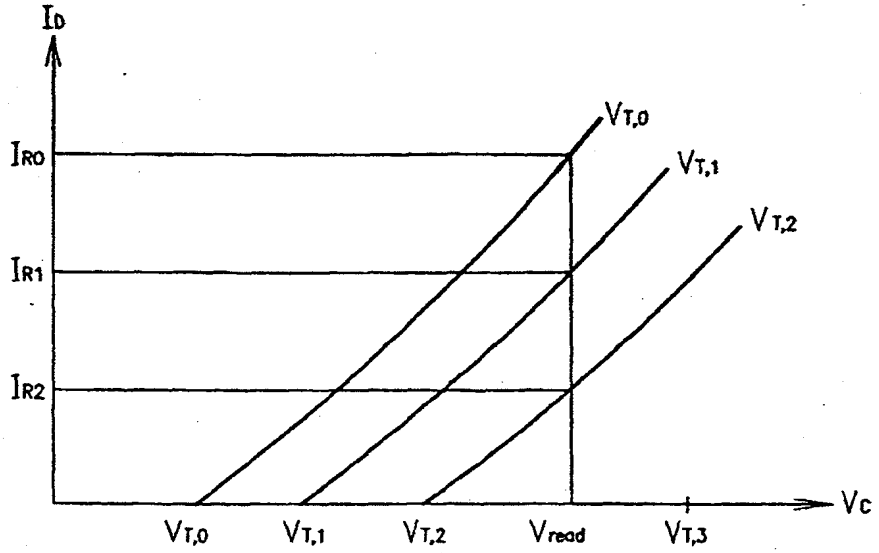

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FIG.3

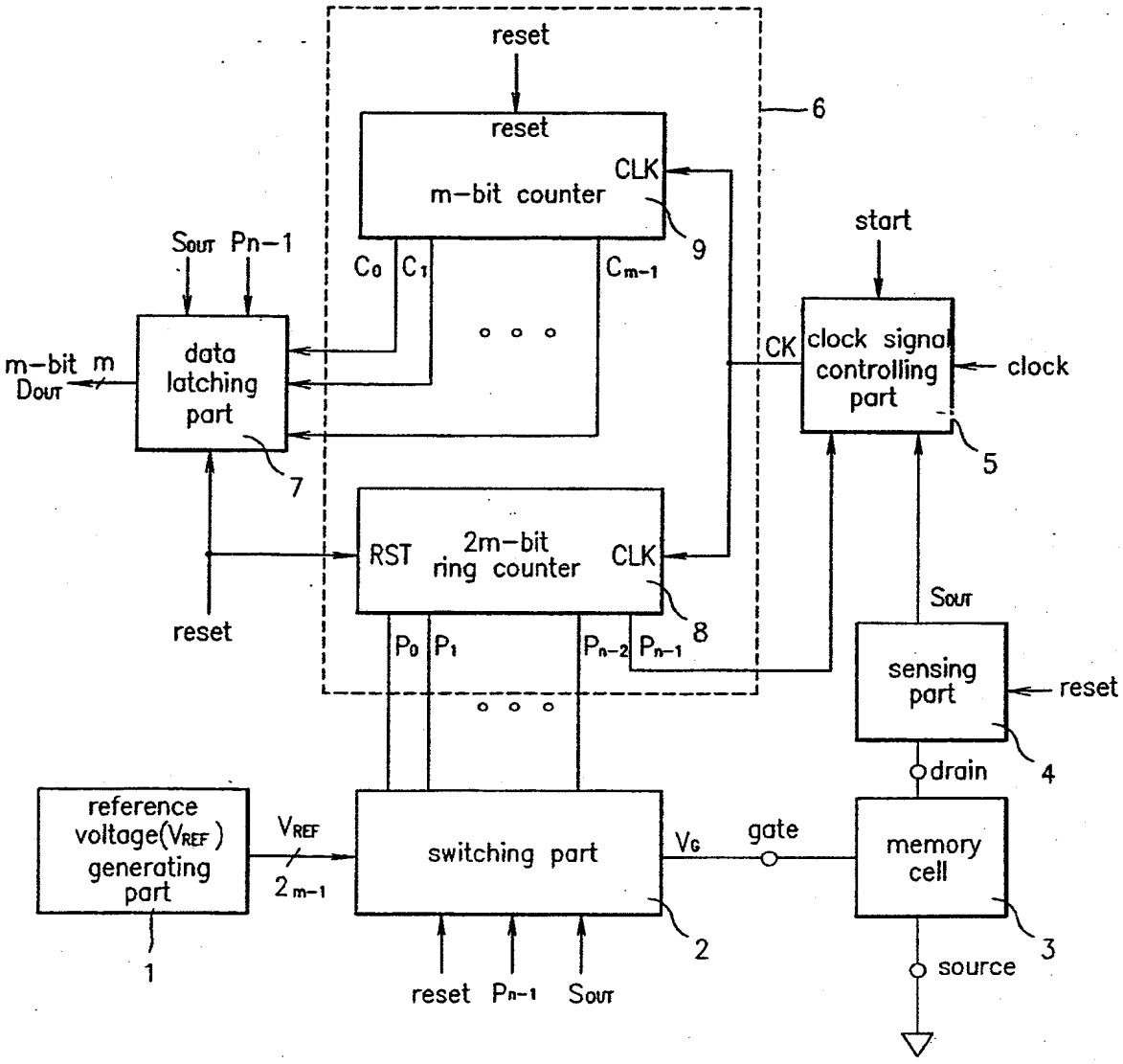

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FIG.4

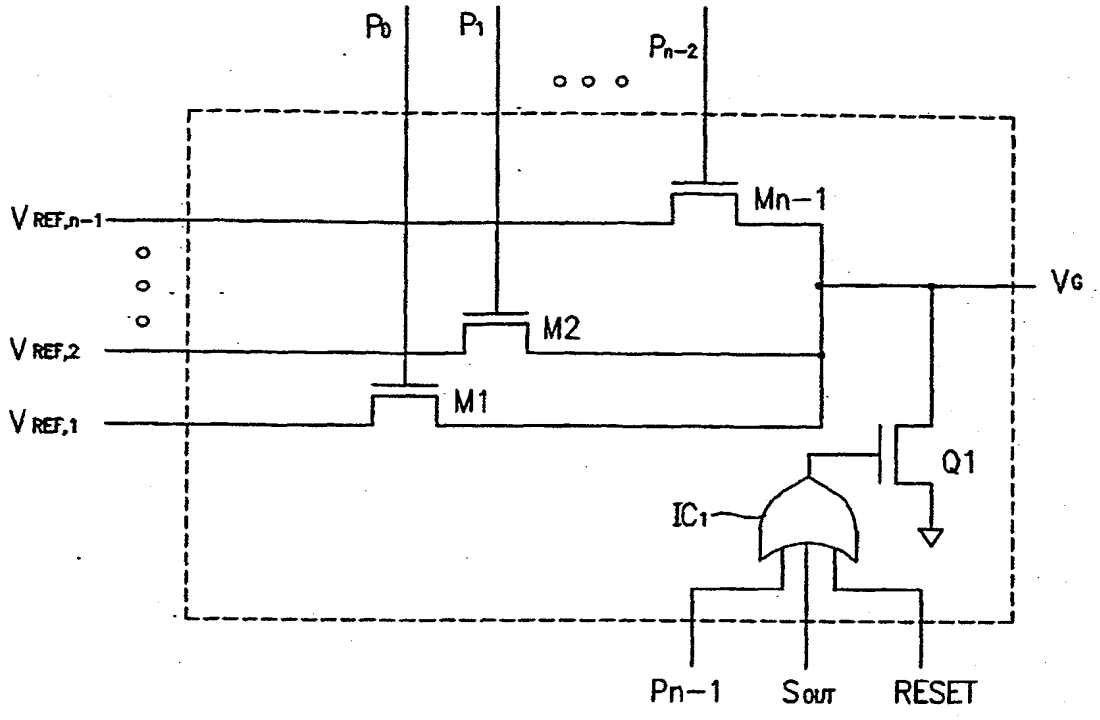

FIG.5

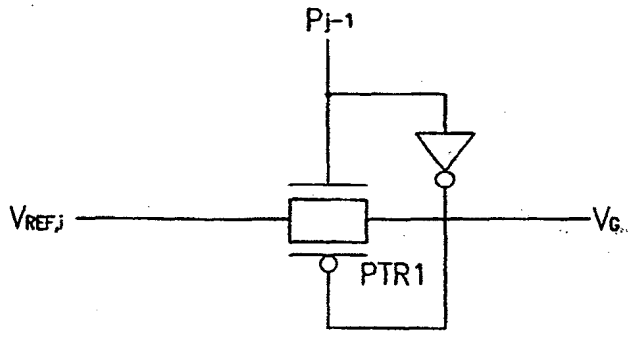

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FIG.6

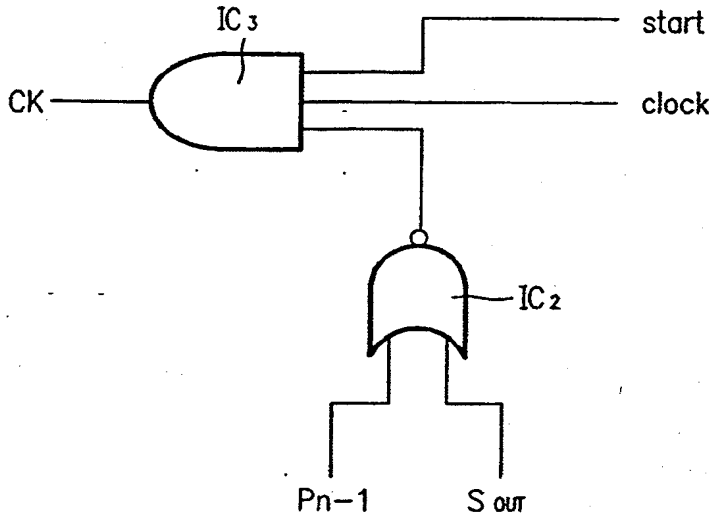

FIG.7

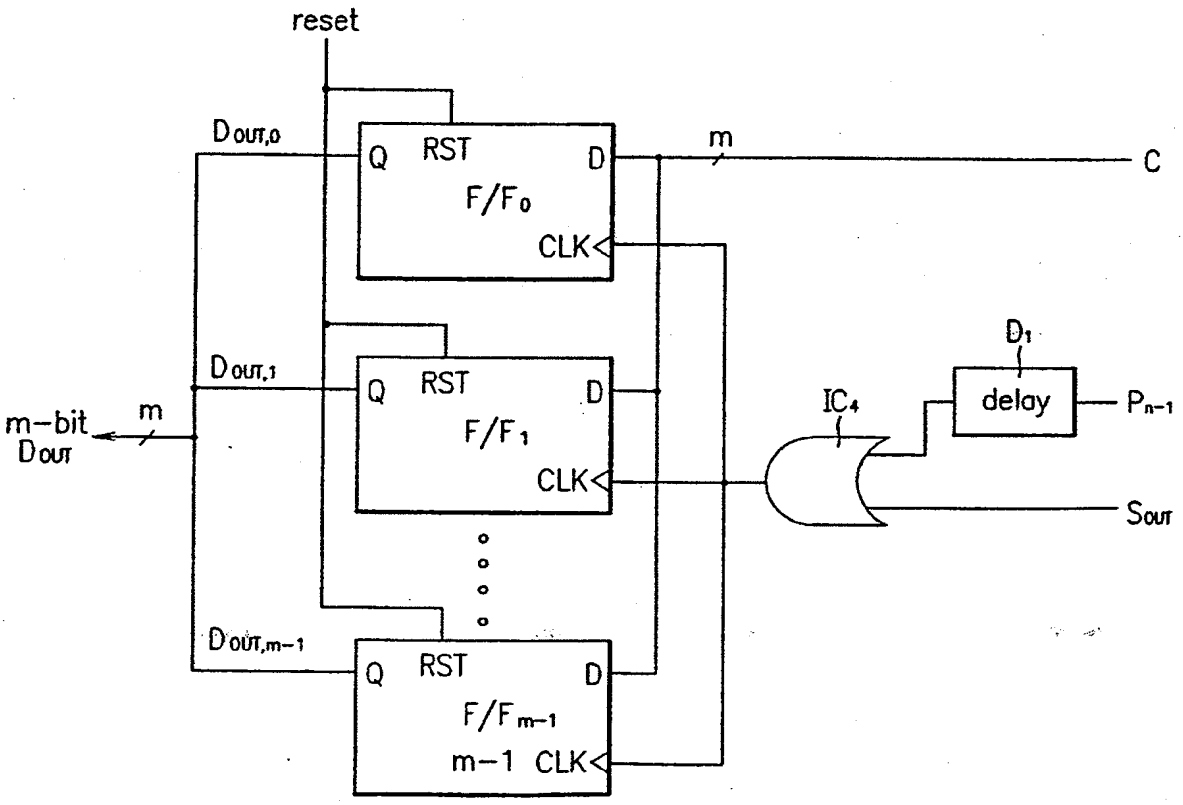

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FIG.8

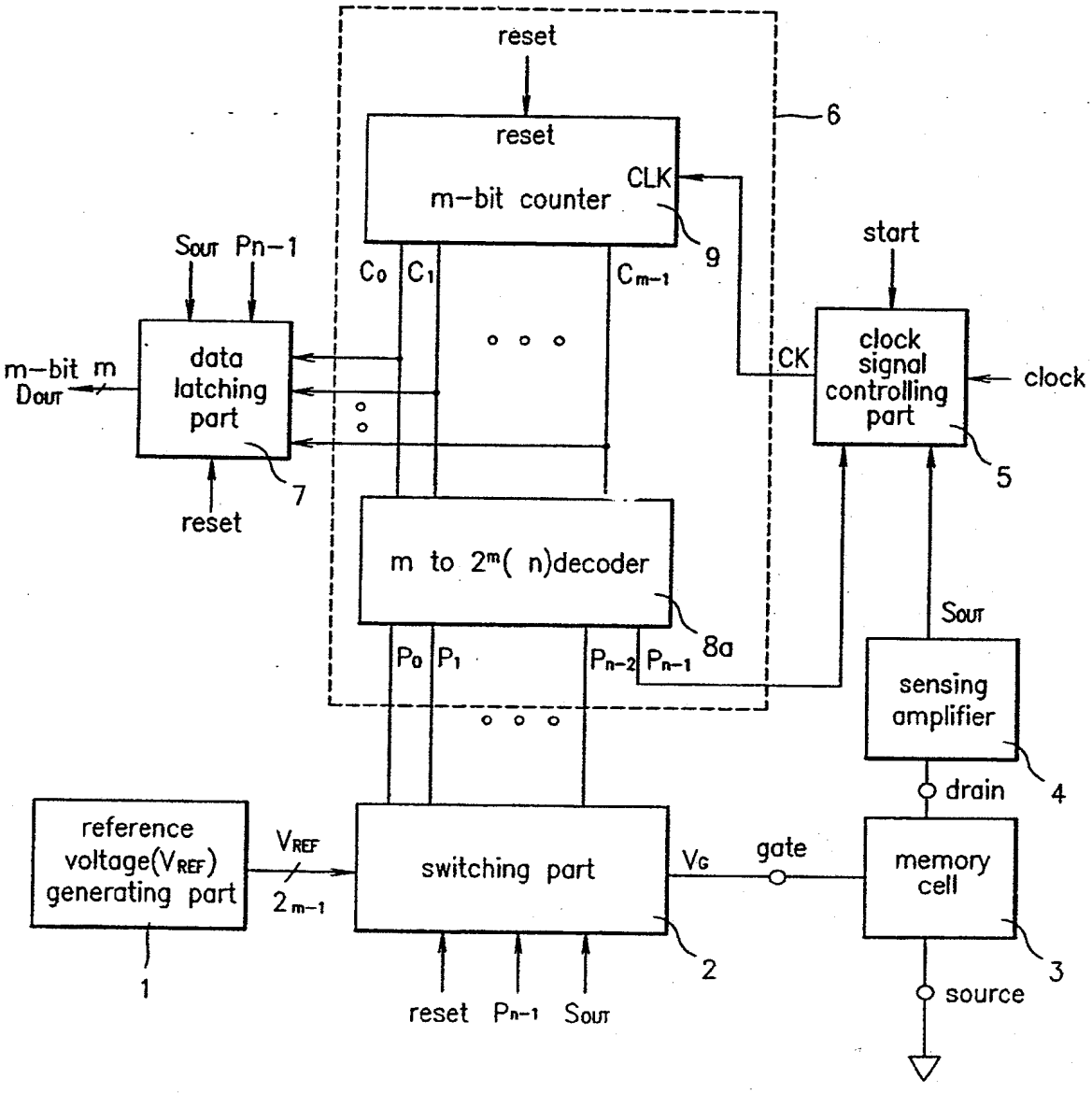

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FIG.9

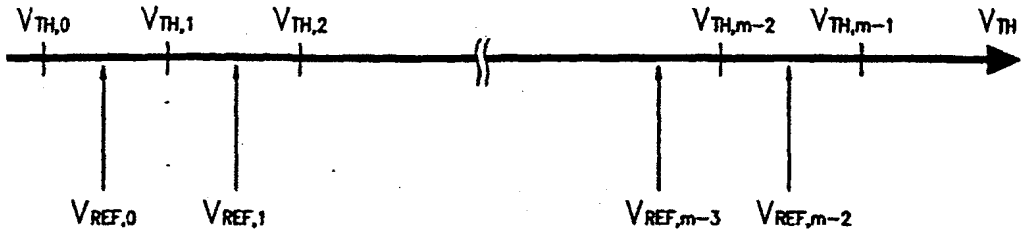

FIG.10

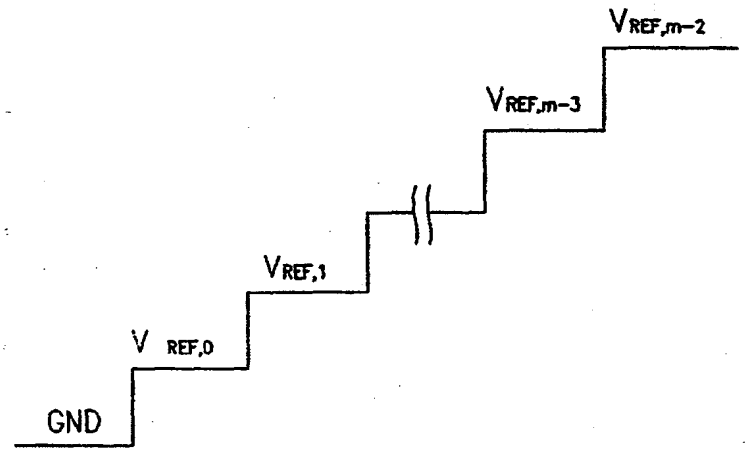

FIG.11

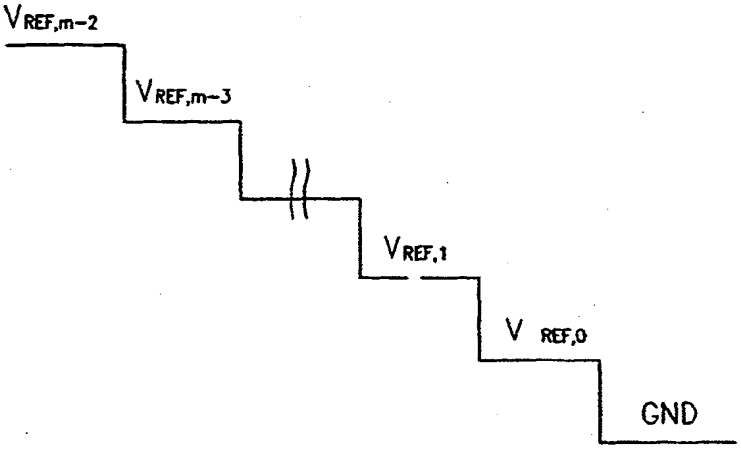

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FIG.12

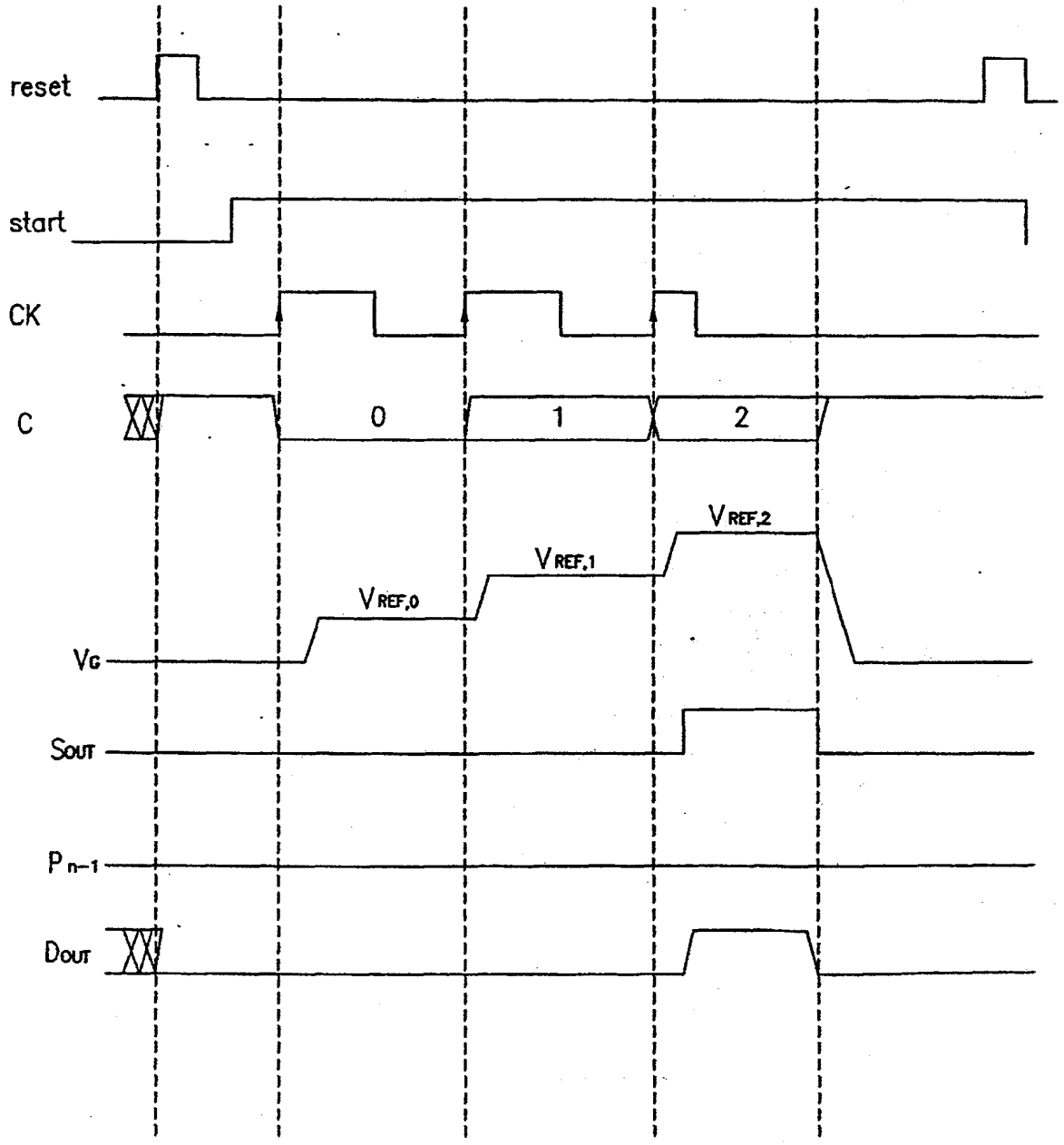

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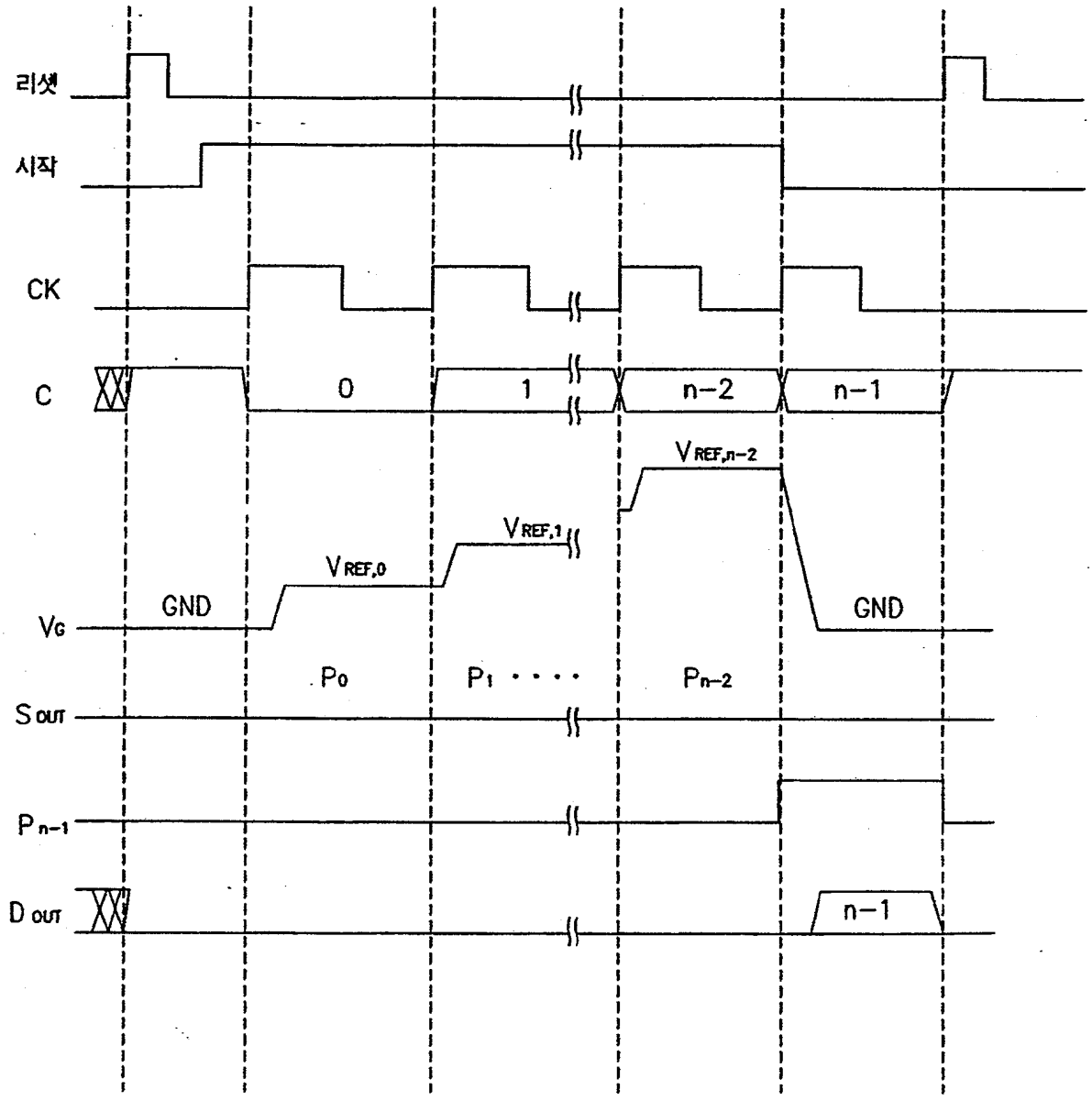
FIG.13



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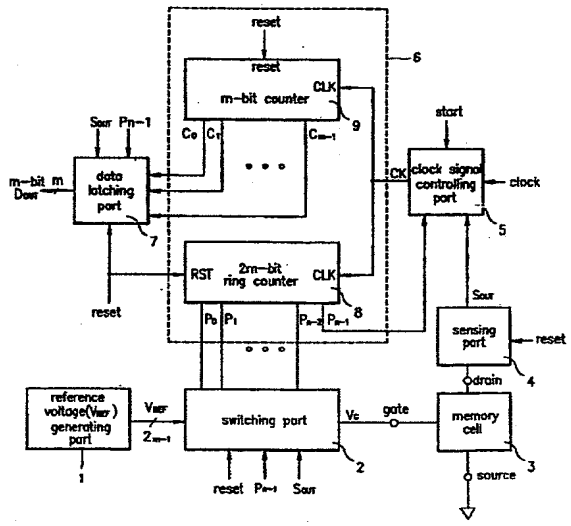
(54) Data sensing device and method for multibit memory cell

(57) Data sensing device and method for a multibit memory cell is disclosed, the device including a reference voltage generating part (1) for generating a plurality of reference voltages, a switching part (2) for successive application of the plurality of reference voltages from the reference voltage generating part (1) to a control gate on a memory cell (3), a sensing part (4) for comparing a data recorded in the memory cell (3) to the reference value every time each of the reference voltages is applied thereto, a clock signal controlling part (5) for subjecting a signal from the sensing part (4) and a highest reference voltage selecting signal to logical operation in controlling an external main clock signal, a controlling part (6) for controlling the switching part (2) to generate the reference voltages in succession, and controlling a highest reference voltage to be applied to the clock signal controlling part (5) so that the data is produced in response to a clock signal from the clock signal controlling part (5), and a latching part (7) for latching the data from the controlling part (6).

FIG.3



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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 10 9419

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 5 508 958 A (FAZIO ALBERT ET AL) 16 April 1996 * abstract; figures 5A,5B,6,9 * ---	1,8	G11C11/56
A	JUNG T -S ET AL: "A 117-MM2 3.3-V ONLY 128-MB MULTILEVEL NAND FLASH MEMORY FOR MASS STORAGE APPLICATIONS" November 1996 , IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 31, NR. 11, PAGE(S) 1575 - 1583 XP000691441 * page 1577, right-hand column, line 33 - page 1578, right-hand column, line 2 * ---	1	
A	US 5 457 650 A (SUGIURA NOBUTAKE ET AL) 10 October 1995 * column 3, line 38 - column 3, line 67; figures 1,8 * ---	1	
P,A	WO 97 13250 A (AGATE SEMICONDUCTOR INC) 10 April 1997 * figures 5,7,8C * -----	5	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 February 1999	Wolff, N

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